REMARKS

This amendment is submitted in response to the Final Office Action dated July 20, 2007. Reconsideration and allowance of the claims are requested. In this Final Office Action, claims 1, 2, 5-11, 14, 31, 33 and 34 are rejected under 35 U.S.C. 102 as anticipated by *Simmonds*, (U.S. 6,646,654.). Claims 12 and 13 are rejected under 35 U.S.C. 103 as unpatentable over *Simmonds*. Claims 3, 4 and 32 are rejected under 35 U.S.C. 103 as unpatentable over *Simmonds* in view of *Deering* (U.S. 2004/0012600). Claim 35 is rejected under 35 U.S.C. 103 as unpatentable over *Simmonds* in view of *Itaki* (U.S. 6,900,844). All these rejections are respectfully traversed.

The independent claims 1 and 31 of the present application recite, in similar language, a method and apparatus for receiving both a clock signal and an external synchronization signal, determining whether the phase of the clock signal, and the phase of the external sync signal are synchronized, adjusting the frequency of a clock generator to the frequency of the external sync signal to generate a synchronized timing signal, transmitting that synchronized signal to another GPU, and utilizing that synchronized signal to produce an image at multiple displays. These limitations, are not found and in the *Simmonds* reference.

The Examiner especially refers to the PLL 130 shown in Figures 4 and 5 of *Simmonds for his rejections*. However, in contrast to the clear statements of the claims summarized above, *Simmonds* teaches that a choice is made at MUX 122 between two possible clock signals to control multiple graphic sub-systems. As clearly shown at Figure 4, the MUX 122 chooses between one of two available clock sources, using the external clock source, if the graphics sub-system is a slave, and the internal clock source from the reference clock oscillator 120, if the system is the master system. There is no connection between the reference clock oscillator and the PLL 130. There is no comparison, as claimed, between the external sync signal and the internal clock oscillator signal 120 to determine if they are in phase. Rather, as clearly shown at Figure 5, there is a master/slave detection mechanism that incorporates the PLL 130. The PLL output chooses the external signal, if it determined that the sync card 100 is a slave, or the reference clock oscillator 120, if the card is the master. *Simmonds* also

does not teach adjusting an internal clock generator's frequency to match in phase an external sync signal to generate a synchronize timing signal. Column 8, lines 50-56 teaches that the PLL can be replaced by a simple switch, that designates a particular card is a master or a slave unit. Therefore, *Simmonds*, while teaching that a card may have both an internal clock and an external reference signal, does not teach a comparison between them or an adjustment of the internal clock based on that comparison.

Claims 3, 4 and 32, which teach synchronizing a first stereo field of the first GPU with a second stereo field of the second GPU must similarly be allowed. The rejection depends entirely on the Examiner's assumption that *Simmonds* teaches adjusting the phase of video signals of the first and second GPU's, which, as demonstrated above, does not occur.

Claim 5 and its dependent claims 6-13 and claim 33 also recite allowable subject matter. The Examiner alleges that *Simmonds* teaches synchronizing a swap ready signal of the first GPU with a swap ready signal of the second GPU (citing Col. 9, lines 56-67 of the reference). In fact, this is contradicted by Col. 10, lines 52-67 of *Simmonds*, which teaches that buffer swap synchronization occurs in a different manner than that claimed. *Simmonds* depends upon a master swap controller connected to all graphics sub-systems that determines that an interrupt has occurred at each graphics sub-system. *Simmonds* teaches a highly inefficient and time consuming process that depends on every GPU being interrupted so that a buffer swap may occur under the direction of a master controller.

In the claimed system, the detection of swap-ready signals between first and second GPUs causes an immediate scan out the data once synchronization occurs. This is a much more efficient and faster approach than that taught by *Simmonds*, the type of approach that is required by high-speed graphics processing to avoid deterioration of the image.

In view of these clear distinctions, reconsideration and allowance of the claims is requested.

Respectfully submitted,

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